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EXAMINER	
WILLIAMS, ALEXANDER O	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,564	CHIANG, CHENG-LIEN	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-100* is/are pending in the application.

4a) Of the above claim(s) *61-90* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60 and 91-100* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/03; 11/6/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS filed 12/22/03 and 1/27/04*.

Serial Number: 10/695564 Attorney's Docket #: BDG005-6
Filing Date: 10/28/03;

Applicant: Chiang

Examiner: Alexander Williams

Applicant's election of the species of figure 19 (claims 1 to 60 and 91 to 100) filed 7/9/04, has been acknowledged.

Applicant's arguments on pages 25 to 27 are not found to be persuasive. The Examiner would be unduly burdened to evaluate all claims fully on their merit at the full time. Applicant's arguments are not found persuasive because of the reasons detailed in the last Office action.

The requirement is still deemed proper and is therefore made FINAL.

This application contains claims 61 to 90 drawn to an invention non-elected with traverse. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR § 1.144 & MPEP § 821.01).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: Applicant's related applications information should be updated.

Appropriate correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, **the first**

semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and **a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad,** wherein the first lead outside the first insulative housing is bent downwardly; a second semiconductor package device, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; **a second semiconductor chip within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad**, wherein the second lead outside the second insulative housing is flat in claims 1, 11, 21, 31, 41, 51, 61 and 91 and stacked device is devoid of wire bonds and TAB leads in claims 10, 20, 40, 50, 60 and 100 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not

be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1 to 60 and 91 to 100 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 11, 21, 31, 41, 51, 61 and 91, it is unclear and confusing to what is meant and what shows "**the first semiconductor chip within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad;** and **a first lead that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad,** wherein the first lead outside the first insulative housing is bent downwardly; a second semiconductor package device, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; **a second semiconductor chip within the second insulative housing, wherein the**

second chip includes a second includes a second conductive pad; and a second lead that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat." Where is this structure show the elected species of figure 19?

In claims 10, 20, 40, 50, 60 and 100, it is unclear and confusing to what is meant by and what shows "stacked device is devoid of wire bonds and TAB leads." Where is this shown in the drawing and what type does this invention relate too since it is not shown in the elected species of figure 19?

Any of claims 1 to 60 and 91 to 100 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 9-16 and 18-20, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Ohuchi et al. (U.S. Patent # 6,084,293).

1. Ohuchi (figures 1 to 17) specifically figure 9 show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **3,** comprising: a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip **(within 3)** within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad (inherit); and a first lead **41** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly; a second semiconductor package device **40**, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(within 40)** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface,, and the second upper surface includes a second conductive pad; and a second lead **21** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat; and a conductive bond **42** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the leads; wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the

insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.
2. The stacked device of claim 1, Ohuchi show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.
3. The stacked device of claim 1, Ohuchi show wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.
4. The stacked device of claim 1, Ohuchi show wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.
5. The stacked device of claim 1, Ohuchi show wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner comer, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.
6. The stacked device of claim 5, Ohuchi show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.
7. The stacked device of claim 1, Ohuchi show wherein the conductive bond is spaced from the insulative housings.
9. The stacked device of claim 1, Ohuchi show wherein the conductive bond has a substantially spherical shape.
10. The stacked device of claim 1, Ohuchi show wherein the stacked device is devoid of wire bonds and TAB leads as much as Applicant does.
11. Ohuchi (figures 1 to 17) specifically figure 9 show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **3**, comprising: a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip (within 3) within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and a first

lead **41** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad (inherit), wherein the first lead outside the first insulative housing is bent downwardly, extends laterally from the first peripheral side surface a first distance, and extends downwardly beyond the first bottom surface; a second semiconductor package device **40**, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip (within 40) within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad (inherit); and a second lead **21** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat, extends laterally from the second peripheral side surface a second distance, and does not extend downwardly beyond the second bottom surface; and a conductive bond **42** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the leads; wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the leads do not contact any insulative material of the stacked device outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, and the first distance is greater than the second distance.

12. The stacked device of claim 11, Ohuchi show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

13. The stacked device of claim 11, Ohuchi show wherein the insulative housings are essentially identical to and vertically aligned with one another.

14. The stacked device of claim 11, Ohuchi show wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

15. The stacked device of claim 11, Ohuchi show wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner comer, a sloped

portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

16. The stacked device of claim 15, Ohuchi show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

18. The stacked device of claim 11, Ohuchi show wherein the conductive bond contacts only the leads.

19. The stacked device of claim 11, Ohuchi show wherein the conductive bond has a substantially spherical shape.

20. The stacked device of claim 11, Ohuchi show wherein the stacked device is devoid of wire bonds and TAB leads as much as Applicant does.

Claims 1-6, 8, 11, 12, 14-18, 91-96 and 98, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Choi (U.S. Patent # 6,190,944 B1).

1. Choi (figures 3A to 7E) specifically figure 3A show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **P1,** comprising: a first insulative housing **36** with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip **(31 within P1)** within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad **(32 within P1)**; and a first lead **33** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly; a second semiconductor package device **P2**, comprising: a second insulative housing **136** with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(31 with P2)** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad **(32 with P2)**; and a second lead **133b** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat; and a

conductive bond **30** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the leads; wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

2. The stacked device of claim 1, Choi show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

3. The stacked device of claim 1, Choi show wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

4. The stacked device of claim 1, Choi show wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

5. The stacked device of claim 1, Choi show wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

6. The stacked device of claim 5, Choi show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

8. The stacked device of claim 1, Choi show wherein the conductive bond is outside the peripheries of the insulative housings.

11. Choi (figures 3A to 7E) specifically figure 3A show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **P1**, comprising: a first insulative housing **36** with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip **(31 within P1)** within the first insulative housing, wherein the first chip includes a first upper surface and a

first lower surface, and the first upper surface includes a first conductive pad; and a first lead **33** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad **(32 within P1)**, wherein the first lead outside the first insulative housing is bent downwardly, extends laterally from the first peripheral side surface a first distance, and extends downwardly beyond the first bottom surface; a second semiconductor package device **P2**, comprising: a second insulative housing **136** with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(31 within P2)** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad **(31 within P2)**; and a second lead **133b** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat, extends laterally from the second peripheral side surface a second distance, and does not extend downwardly beyond the second bottom surface; and a conductive bond **30** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the leads; wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the leads do not contact any insulative material of the stacked device outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, and the first distance is greater than the second distance.

12. The stacked device of claim 11, Choi show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

14. The stacked device of claim 11, Choi show wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

15. The stacked device of claim 11, Choi show wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner comer, a sloped

portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

16. The stacked device of claim 15, Choi show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

17. The stacked device of claim 11, Choi show wherein the conductive bond is spaced from the insulative housings and outside the peripheries of the insulative housings.

18. The stacked device of claim 11, Choi show wherein the conductive bond contacts only the leads.

91. Choi (figures 3A to 7E) specifically figure 3A show a method of making a three-dimensional stacked semiconductor package device, comprising: providing a first semiconductor package device **P1** that includes a first insulative housing **36**, a first semiconductor chip **(31 in P1)** and a first lead **33**, wherein the first insulative housing includes a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces, the first chip is within the first insulative housing, the first chip includes a first upper surface and a first lower surface, the first upper surface includes a first conductive pad **(32 within P1)**, and the first lead protrudes laterally from and extends through the first peripheral side surface, is electrically connected to the first pad and is flat outside the first insulative housing; providing a second semiconductor package device **P2** that includes a second insulative housing **136**, a second semiconductor chip **(31 within P2)** and a second lead **133b**, wherein the second insulative housing includes a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces, the second chip is within the second insulative housing, the second chip includes a second upper surface and a second lower surface, the second upper surface includes a second conductive pad **(32 within P2)**, and the second lead protrudes laterally from and extends through the second peripheral side surface, is electrically connected to the second pad and is flat outside the second insulative housing; bending the first lead downwardly outside the first insulative housing; then positioning the first and second devices so that the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom

surfaces face downwardly, and the first top surface faces towards the second bottom surface; and electrically connecting the leads using a conductive bond **30** that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts the leads outside the insulative housings, wherein the first lead remains bent and the second lead remains flat outside the insulative housings.

92. The method of claim 91, Choi show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

93. The method of claim 91, Choi show wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

94. The method of claim 91, Choi show wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

95. The method of claim 91, Choi show wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

96. The method of claim 95, Choi show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

98. The method of claim 91, Choi show wherein the conductive bond is outside the peripheries of the insulative housings.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a second lead and a conductive bond deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1-8, 11-18, 31-39, 41-48, 51-58 and 91-98, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kang (U.S. Patent # 6,242,285 B1).

1. Kang (figures 2A to 7B) specifically figures 4A and 4B show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **IC(sub A),** comprising: a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip **(inherit within IC(sub A))** within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad (inherit); and a first lead **(P1(sub A)-P27(sub A))** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first

insulative housing is bent downwardly; a second semiconductor package device **(IC(sub B))**, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(inherit within IC(sub B))** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and a second lead **{upper flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B))}** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat; and a conductive bond **{side flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B)) and 70}** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the leads; wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

2. The stacked device of claim 1, Kang show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

3. The stacked device of claim 1, Kang show wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

4. The stacked device of claim 1, Kang show wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

5. The stacked device of claim 1, Kang show wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between

the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

6. The stacked device of claim 5, Kang show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

7. The stacked device of claim 1, Kang show wherein the conductive bond is spaced from the insulative housings.

8. The stacked device of claim 1, Kang show wherein the conductive bond is outside the peripheries of the insulative housings.

11. Kang (figures 2A to 7B) specifically figures 4A and 4B show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **IC(sub A)**, comprising: a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip **(inherit within IC(sub A))** within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad (inherit); and a first lead **(P1(sub A)-P27(sub A))** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad (inherit), wherein the first lead outside the first insulative housing is bent downwardly, extends laterally from the first peripheral side surface a first distance, and extends downwardly beyond the first bottom surface; a second semiconductor package device **(IC(sub B))**, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(inherit within IC(sub B))** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad (inherit); and a second lead **{upper flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B))}** that protrudes laterally from and the second peripheral side surface a second distance, and does not extend downwardly beyond the second bottom surface; and a conductive bond **{side flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B)) and 70}** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts and electrically connects the

leads; wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the leads do not contact any insulative material of the stacked device outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, and the first distance is greater than the second distance.

12. The stacked device of claim 11, Kang show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

13. The stacked device of claim 11, Kang show wherein the insulative housings are essentially identical to and vertically aligned with one another.

14. The stacked device of claim 11, Kang show wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

15. The stacked device of claim 11, Kang show wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner comer, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.

16. The stacked device of claim 15, Kang show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

17. The stacked device of claim 11, Kang show wherein the conductive bond is spaced from the insulative housings and outside the peripheries of the insulative housings.

18. The stacked device of claim 11, Kang show wherein the conductive bond contacts only the leads.

31. Kang (figures 2A to 7B) specifically figures 4A and 4B show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **IC(sub A)**, comprising: a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip **(inherit within IC(sub A))** within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface

includes a first conductive pad (inherit); and a first lead **(P1(sub A)-P27(sub A))** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a first distal end; a second semiconductor package device **IC(sub B)**, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(inherit within IC(sub B))** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad (inherit); and a second lead **{upper flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B))}** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat and extends laterally between the second peripheral side surface and a second distal end; and a conductive bond **{side flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B)) and 70}** outside the insulative housings and outside the peripheries of the insulative housings that extends laterally beyond any insulative material of the stacked device, contacts and electrically connects the leads and does not contact any other material; wherein the insulative housings are essentially identical to and vertically aligned with one another, the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

32. The stacked device of claim 31, Kang show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

33. The stacked device of claim 31, Kang show wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

34. The stacked device of claim 31, Kang show wherein the second corner laterally extends a first distance from the first peripheral side surface, the second distal end laterally extends a second distance from the second peripheral side surface, and the first distance is greater than the second distance.
35. The stacked device of claim 31, Kang show wherein the first corner laterally extends a first distance from the first peripheral side surface, the second distal end laterally extends a second distance from the second peripheral side surface, and the first and second distances are essentially identical.
36. The stacked device of claim 31, Kang show wherein the conductive bond is laterally aligned with the second bottom surface.
37. The stacked device of claim 31, Kang show wherein the conductive bond is closer to the second bottom surface than to the first bottom surface.
38. The stacked device of claim 31, Kang show wherein the conductive bond contacts only the inner lateral portion and the second lead.
41. Kang (figures 2A to 7B) specifically figures 4A and 4B show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **IC(sub A)**, comprising: a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces; a first semiconductor chip **(inherit within IC(sub A))** within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad; and a first lead **(P1(sub A)-P27(sub A))** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly and extends downwardly beyond the first bottom surface; a second semiconductor package device **(IC(sub B))**, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(inherit within IC(sub B))** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad (inherit); and a second lead **{upper flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B))}** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the

second insulative housing is flat; and a conductive bond **{side flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B)) and 70}** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, does not overlap any insulative material of the stacked device, is not overlapped by any insulative material of the stacked device and contacts and electrically connects the leads; wherein the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface.

42. The stacked device of claim 41, Kang show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

43. The stacked device of claim 41, Kang show wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.

44. The stacked device of claim 41, Kang show wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer comers, and an outer lateral portion that extends laterally between the outer corner and a distal end.

45. The stacked device of claim 44, Kang show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.

46. The stacked device of claim 41, Kang show wherein the conductive bond is laterally aligned with the second bottom surface, and is not laterally aligned with the first bottom surface.

47. The stacked device of claim 41, Kang show wherein the conductive bond does not contact any insulative material of the stacked device.

48. The stacked device of claim 41, Kang show wherein the conductive bond contacts only the leads.

51. Kang (figures 2A to 7B) specifically figures 4A and 4B show a three-dimensional stacked semiconductor package device, comprising: a first semiconductor package device **IC(sub A)**, comprising: a first insulative housing with a first top surface, a first bottom surface, and a first peripheral side surface

between the first top and bottom surfaces; a first semiconductor chip **(inherit within IC(sub A))** within the first insulative housing, wherein the first chip includes a first upper surface and a first lower surface, and the first upper surface includes a first conductive pad (inherit); and a first lead **(P1(sub A)-P27(sub A))** that protrudes laterally from and extends through the first peripheral side surface and is electrically connected to the first pad, wherein the first lead outside the first insulative housing is bent downwardly, extends laterally from the first peripheral side surface a first distance, extends downwardly beyond the first bottom surface, does not overlap any insulative material of the first device and is not overlapped by any insulative material of the first device; a second semiconductor package device **(IC(sub B))**, comprising: a second insulative housing with a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces; a second semiconductor chip **(inherit within IC(sub B))** within the second insulative housing, wherein the second chip includes a second upper surface and a second lower surface, and the second upper surface includes a second conductive pad; and a second lead **{upper flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B))}** that protrudes laterally from and extends through the second peripheral side surface and is electrically connected to the second pad, wherein the second lead outside the second insulative housing is flat, extends laterally from the second peripheral side surface a second distance, does not extend downwardly beyond the second bottom surface, does not overlap any insulative material of the second device and is not overlapped by any insulative material of the second device; and a conductive bond **{side flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B)) and 70}** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, does not overlap any insulative material of the stacked device, is not overlapped by any insulative material of the stacked device, extends laterally beyond the first peripheral side surface a third distance and contacts and electrically connects the leads; wherein the insulative housings are essentially identical to and vertically aligned with one another, the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, the first top surface faces towards the second bottom surface, and the first distance is greater than the second and third distances.

52. The stacked device of claim 51, Kang show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.
53. The stacked device of claim 51, Kang show wherein the first lead is adjacent to the first bottom surface, and the second lead is adjacent to the second bottom surface.
54. The stacked device of claim 51, Kang show wherein the first lead includes inner and outer corners that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the inner and outer comers, and an outer lateral portion that extends laterally between the outer comer and a distal end.
55. The stacked device of claim 54, Kang show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.
56. The stacked device of claim 51, Kang show wherein the conductive bond is laterally aligned with the second bottom surface, and is not laterally aligned with the first bottom surface.
57. The stacked device of claim 51, Kang show wherein the conductive bond does not contact any insulative material of the stacked device.
58. The stacked device of claim 51, Kang show wherein the conductive bond contacts only the leads.
91. Kang (figures 2A to 7B) specifically figures 4A and 4B show a method of making a three-dimensional stacked semiconductor package device, comprising: providing a first semiconductor package device **IC(sub A)** that includes a first insulative housing, a first semiconductor chip **(inherit within IC(sub A))** and a first lead **(P1(sub A)-P27(sub A))**, wherein the first insulative housing includes a first top surface, a first bottom surface, and a first peripheral side surface between the first top and bottom surfaces, the first chip is within the first insulative housing, the first chip includes a first upper surface and a first lower surface, the first upper surface includes a first conductive pad (inherit), and the first lead protrudes laterally from and extends through the first peripheral side surface, is electrically connected to the first pad and is flat outside the first insulative housing; providing a second semiconductor package device **(IC(sub B))** that includes a second insulative housing, a second semiconductor chip

(inherit within IC(sub B)) and a second lead **{upper flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B))}**, wherein the second insulative housing includes a second top surface, a second bottom surface, and a second peripheral side surface between the second top and bottom surfaces, the second chip is within the second insulative housing, the second chip includes a second upper surface and a second lower surface, the second upper surface includes a second conductive pad (inherit), and the second lead protrudes laterally from and extends through the second peripheral side surface, is electrically connected to the second pad and is flat outside the second insulative housing; bending the first lead downwardly outside the first insulative housing; then positioning the first and second devices so that the second insulative housing overlaps the first insulative housing, the second lead overlaps the first lead outside the insulative housings, the top surfaces face upwardly, the bottom surfaces face downwardly, and the first top surface faces towards the second bottom surface; and electrically connecting the leads using a conductive bond **{side flat portion (P1(sub B)-P18(sub B)) and (P19(sub B)-P27(sub B)) and 70}** that extends laterally beyond any insulative material of the stacked device, extends downwardly beyond a surface of the first chip and contacts the leads outside the insulative housings, wherein the first lead remains bent and the second lead remains flat outside the insulative housings.

92. The method of claim 91, Kang show wherein the first upper surface faces towards the first bottom surface, and the second upper surface faces towards the second bottom surface.

93. The method of claim 91, Kang show wherein the first lead extends downwardly beyond the first bottom surface outside the first insulative housing, and the second lead does not extend downwardly beyond the second bottom surface outside the second insulative housing.

94. The method of claim 91, Kang show wherein the first lead extends laterally from the first peripheral side surface a first distance, the second lead extends laterally from the second peripheral side surface a second distance, and the first distance is greater than the second distance.

95. The method of claim 91, Kang show wherein the first lead outside the first insulative housing includes inner and outer comers that are bent, an inner lateral portion that extends laterally between the first peripheral side surface and the inner corner, a sloped portion that extends laterally and downwardly between the

inner and outer corners, and an outer lateral portion that extends laterally between the outer corner and a distal end.
96. The method of claim 95, Kang show wherein the second lead outside the second insulative housing is essentially identical to the inner lateral portion of the first lead.
97. The method of claim 91, Kang show wherein the conductive bond is spaced from the insulative housings.
98. The method of claim 91, Kang show wherein the conductive bond is outside the peripheries of the insulative housings.

Therefore, it would have been obvious to one of ordinary skill in the art to use **the second lead and a conductive bond** as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 9, 19, 39, 49, 59 and 99, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kang (U.S. Patent # 6,242,285 B1) in view of Yamazaki et al. (U.S. Patent Application Publication # 2001/0054762 A1).

Kang show the features of the claimed invention as detailed above, but fail to explicitly show the conductive bond has a substantially spherical shape.

Yamazaki et al. Is cited for showing a semiconductor device. Specifically, Yamazaki et al. (figures 3 to 8B) specifically figure 7 discloses a stacked device comprises a conductive bond **7** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, wherein the conductive bond has a substantially spherical shape for the purpose of providing electrical conductions to a vertical stacked semiconductor device.
9, 19, 39, 49, 59 and 99. In method of claim independent claims, the combination with Yamazaki et al show wherein the conductive bond has a substantially spherical shape.

Therefore, it would have been obvious to one of ordinary skill in the art to use Yamazaki et al.'s spherical shape conductive bond to modify Kang's conductive bond combination for the purpose of providing electrical conductions to a vertical stacked semiconductor device.

Claims 9, 19, 39, 49, 59 and 99, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi (U.S. Patent # 6,190,944 B1) in view of Yamazaki et al. (U.S. Patent Application Publication # 2001/0054762 A1).

Choi show the features of the claimed invention as detailed above, but fail to explicitly show the conductive bond has a substantially spherical shape.

Yamazaki et al. Is cited for showing a semiconductor device. Specifically, Yamazaki et al. (figures 3 to 8B) specifically figure 7 discloses a stacked device comprises a conductive bond **7** outside the insulative housings that extends laterally beyond any insulative material of the stacked device, wherein the conductive bond has a substantially spherical shape for the purpose of providing electrical conductions to a vertical stacked semiconductor device.

9, 19, 39, 49, 59 and 99. In method of claim independent claims, the combination with Yamazaki et al show wherein the conductive bond has a substantially spherical shape.

Therefore, it would have been obvious to one of ordinary skill in the art to use Yamazaki et al.'s spherical shape conductive bond to modify Choi's conductive bond combination for the purpose of providing electrical conductions to a vertical stacked semiconductor device.

Claims 10, 20, 40, 50, 60 and 100, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohuchi et al. (U.S. Patent # 6,084,293) in view of Osawa (Japan Patent # 06-097352).

Ohuchi et al. show the features of the claimed invention as detailed above, but fail to explicitly show the stacked device is devoid of wire bonds and TAB leads.

Osawa is cited for showing a resin sealed semiconductor device. Specifically, Osawa (figures 1A to 5B) specifically figures 1A and 1B discloses a semiconductor device that is devoid of wire bonds and TAB leads for the purpose of preventing short circuit between an inner lead and the edge of a semiconductor chip.

10, 20, 40, 50, 60 and 100. In method of independent claims, the combination with Osawa showing a device that is devoid of wire bonds and TAB leads.

Therefore, it would have been obvious to one of ordinary skill in the art to use Osawa's device to modify Ohuchi et al.'s device for the purpose of

preventing short circuit between an inner lead and the edge of a semiconductor chip.

Claims 10, 20, 40, 50, 60 and 100, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over over Kang (U.S. Patent # 6,242,285 B1) in view of Osawa (Japan Patent # 06-097352).

Kang show the features of the claimed invention as detailed above, but fail to explicitly show the stacked device is devoid of wire bonds and TAB leads.

Osawa is cited for showing a resin sealed semiconductor device. Specifically, Osawa (figures 1A to 5B) specifically figures 1A and 1B discloses a semiconductor device that is devoid of wire bonds and TAB leads for the purpose of preventing short circuit between an inner lead and the edge of a semiconductor chip.

10, 20, 40, 50, 60 and 100. In method of independent claims, the combination with Osawa showing a device that is devoid of wire bonds and TAB leads.

Therefore, it would have been obvious to one of ordinary skill in the art to use Osawa's device to modify Kang's device for the purpose of preventing short circuit between an inner lead and the edge of a semiconductor chip.

Claims 10, 20, 40, 50, 60 and 100, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi (U.S. Patent # 6,190,944 B1) in view of Osawa (Japan Patent # 06-097352).

Choi show the features of the claimed invention as detailed above, but fail to explicitly show the stacked device is devoid of wire bonds and TAB leads.

Osawa is cited for showing a resin sealed semiconductor device. Specifically, Osawa (figures 1A to 5B) specifically figures 1A and 1B discloses a semiconductor device that is devoid of wire bonds and TAB leads for the purpose of preventing short circuit between an inner lead and the edge of a semiconductor chip.

10, 20, 40, 50, 60 and 100. In method of independent claims, the combination with Osawa showing a device that is devoid of wire bonds and TAB leads.

Therefore, it would have been obvious to one of ordinary skill in the art to use Osawa's device to modify Choi's device for the purpose of preventing short circuit between an inner lead and the edge of a semiconductor chip.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/777,723,686,685,734,737,738,673,676,691,696,698, 784,786,666,775,776,680,774,692,693,779,678,688	8/26/04
Other Documentation: foreign patents and literature in 257/777,723,686,685,734,737,738,673,676,691,696,698, 784,786,666,775,776,680,774,692,693,779,678,688	8/26/04
Electronic data base(s): U.S. Patents EAST	8/26/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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AOW
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